IN THE TITLE:

Please delete the existing title and substitute therefor PROCESSOR EXECUTION, PIPLELINE SHARING INSTRUCTION, AND DATA SOURCE PATH.

IN THE SPECIFICATION:

The specification as amended below with replacement paragraphs shows added text with underlining and deleted text with ~~strikethrough~~.

Please REPLACE the paragraph beginning at page 1, line 14, with the following paragraph:

A2

As microprocessors that achieve high-speed processing, pipeline operators that use pipeline processing have been used. The pipeline processing employs a method of overlapping the processing of a plurality of instructions by delaying the starting time of the execution of each instruction one clock by one clock, thereby achieving the execution of the instructions at an equivalent high speed. Before installing a pipeline operator into a computer system, the installation area, power consumption, and price of the pipeline operator are important factors that need to be examined. The pipeline operator must meet compactness, low power consumption, and low price as essential conditions.

Please REPLACE the paragraph beginning at page 8, line 4, with the following paragraph:

A3

According to the conventional pipeline operator, because the stage latch circuit 11, and the stage latch circuit 21_2 are provided independent of each other between the first processing stage and the second processing stage, as explained above, the circuits (the stage latch circuits, the wiring and the control circuits) have redundant structures. Accordingly, the conventional pipeline operator poses a problem because it requires a large scale of hardware , and as a result has high power consumption.

Please REPLACE the paragraph beginning at page 13, line 13, with the following paragraph:

A4

As explained above, according to the third aspect, the processing data held in the upstream latching units are passed through the first processing unit to the (x-1)-th processing unit at the time of decoding the instruction to the x-th processing unit. Therefore, it is possible to reduce both the stage latch circuits and the wiring at the first processing stage to the (x-1)-th processing stage in comparison to the conventional levels. As a result, the hardware volume and power consumption can be reduced.

Please REPLACE the paragraph beginning at page 15, line 8, with the following paragraph:

A5

As explained above, according to the fourth aspect, the processing result of the x-th latching unit held in the upstream latching unit is passed through the (x+1) -th processing unit to the n-th processing unit at the time of decoding instruction to the x-th processing unit. Therefore, it is possible to reduce both the stage latch circuits and the wiring needed in the (x+1) -th processing unit to the n-th processing stage in comparison to the conventional levels. As a result, the hardware volume and power consumption can be reduced.